

ZERO VOLTAGE TRANSITION SYNCHRONOUS RECTIFIER BUCK CONVERTER

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ABSTRACT

This paper proposes a zero-voltage-transition (ZVT) buck converter with synchronous rectifier (SR). The conduction losses due to rectifying diode can be reduced by SR but the reverse recovery time of SR body diode will increase switching losses and electromagnetic interference (EMI). So soft switching techniques are employed. In this converter zero voltage switching (ZVS) is achieved for main switch and SR. Also zero current switching (ZCS) for auxiliary switch. The ZVT synchronous buck converter is analysed and simulation results are obtained.

KEYWORDS: Buck Converter, Synchronous Rectifier (SR), Zero Voltage Transition (ZVT)

I. INTRODUCTION

Most Power Electronic systems can be simplified into three general components the source, converter, and load. The source provides the input energy and the load uses that energy to perform the desired task. The load can be anything from a motor to a microprocessor or a combination of items. In most systems some form of conversion is needed to provide the load with correct form of energy it needs. Certainly energy savings in any system can be made almost anywhere in the system. The converter, being central to the energy flow, can be one of the best places to reduce unwanted losses. The ideal converter does not have any losses. In any real converter, this is not the case of course and there are losses. Reducing this loss to a minimum is necessary to have a high level of efficiency.

The buck converter is the most widely used dc-dc converter topology in power management and microprocessor voltage-regulator (VRM) applications. Those applications require fast load and line transient responses and high efficiency over a wide load current range. They can convert a voltage source into a lower regulated voltage. Synchronous rectifier can be applied to buck converter to decrease conduction loss of rectifying diode. The reverse recovery time of SR body diode is greater than 150ns which increases switching losses and electromagnetic interferences. Thus soft switching techniques are employed to reduce switching losses and electromagnetic interference (EMI). Soft switching topologies make use of additional circuit elements (passive or active) in order to limit di/dt or dv/dt during switching and minimize current and voltage overlap to reduce switching losses. In the switching device at the switching interval, either the current or the voltage must be driven to zero to bring the product of the two as close to zero as possible. This leads to the concepts of zero voltage switching (ZVS) and zero current switching (ZCS). But these converters can cause some problems such as

additional voltage or current stress on the main switch. Converters that have soft switching but reduce or eliminate this stress are more highly desirable. So zero voltage transition (ZVT) converter are preferred.

In ZVT technique, a capacitor is placed in parallel with the main switch to provide soft switching condition for switch turn-off and soft switching condition for switch turn-on is achieved by an auxiliary switch, which discharges the snubber capacitor across the main switch. Therefore, when the auxiliary switch is turned on in ZVT converters, it first provides the converter inductor current and the converter main diode turns off. Then, the snubber capacitor of main switch is discharged in a resonance fashion. Thus, ZVT techniques create a time gap between the conduction time of the main switch and diode. Thus by applying ZVT techniques to regular converters with synchronous rectifier, the losses related to the reverse recovery time of SR body diode can be reduced significantly and the efficiency is improved.

Several ZVT techniques are introduced to PWM converters with synchronous rectifiers to improve efficiency and to reduce synchronous rectifier reverse recovery problems. Compared with ZVS-PWM converter, zero-voltage-transition PWM converters [3] are more desirable since soft switching is achieved without increasing switch voltage and current stress. In ZCT technique, an inductor is placed in series with converter main switch or main diode to provide soft switching condition at switch turn-on instant. Before switch turn-off instant, an auxiliary switch is turned on and the main switch current is reduced to zero [2]. The advantage of ZVT method over ZCT is the elimination of switch turn-on capacitive losses, which are considerable at high frequencies. ZVT technique in [4] improves efficiency but additional current stress is applied to the main switch. The auxiliary switch voltage stress is also high. In some ZVT technique applied to the PWM converters [7], [8], the efficiency is comparatively reduced as two resonances occurs simultaneously to discharge the snubber capacitor in the auxiliary circuit. In [5], [6], a complete resonance cycle occurs to discharge the snubber capacitor. The ZVT technique in [4] has better efficiency but it can provide zero voltage switching at operating duty cycles higher than 0.5. This paper presents a new ZVT technique for synchronous buck converter that increases efficiency and soft switching range.

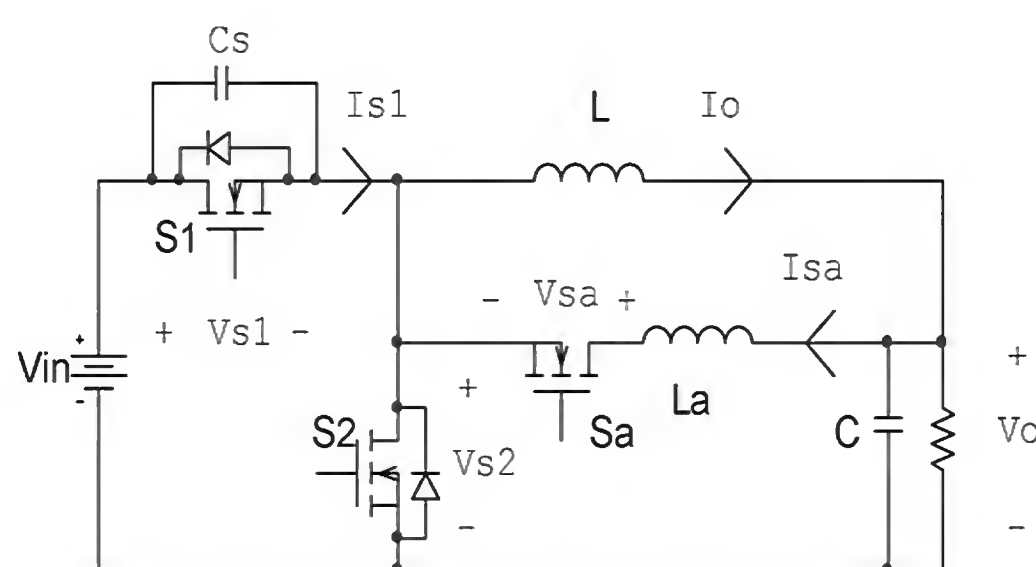


Figure 1: ZVT Buck Converter with SR

In this paper the circuit topology and operation principle for the ZVT buck converter with synchronous rectifier is explained in Section II. The design procedure of the proposed circuit is introduced in Section III. Section IV of the paper presents the simulation results and efficiency comparison of this proposed converter with conventional buck converter and synchronous buck converter. Finally, the conclusion is given in Section V.

II. PRINCIPLE OF OPERATION

Figure 1 shows the proposed ZVT buck converter with synchronous rectifier. The converter is composed of main switch S1, synchronous rectifier switch S2, output filter inductor L and output filter capacitor C . The auxiliary circuit is composed of unidirectional auxiliary switch S_a and auxiliary inductor L_a . C_s is the snubber capacitor of main switch.

For converter analysis, all semiconductor devices are assumed ideal. Also, inductor L current and input voltage are assumed constant in a switching cycle, and are equal to I_o and V_{in} , respectively. Main theoretical waveforms are shown in Figure 2. Equivalent circuit for each operating interval is presented in Figure 3. Before the first interval, it is assumed that S2 is conducting current I_o and all other semiconductor devices are OFF.

Interval 1 [$t_0 - t_1$]: This interval starts by turning the auxiliary switch S_a on, thus the output voltage is placed across L_a and current through L_a increases linearly to I_o . S2 current decreases from I_o to zero, respectively. Due to L_a , S_a turns on under zero current switching (ZCS).

Interval 2 [$t_1 - t_2$]: In this interval, S2 is ON, and thus, L_a current increases linearly from I_o to its maximum value at the end of this interval. This additional energy stored in L_a is used to discharge the snubber capacitor.

Interval 3 [$t_2 - t_3$]: This interval starts by turning S2 off. Thus, a resonance begins between L_a and C_s . By the end of this interval, C_s is completely discharged. Due to the existence of C_s , S2 turn-OFF is under zero voltage switching (ZVS).

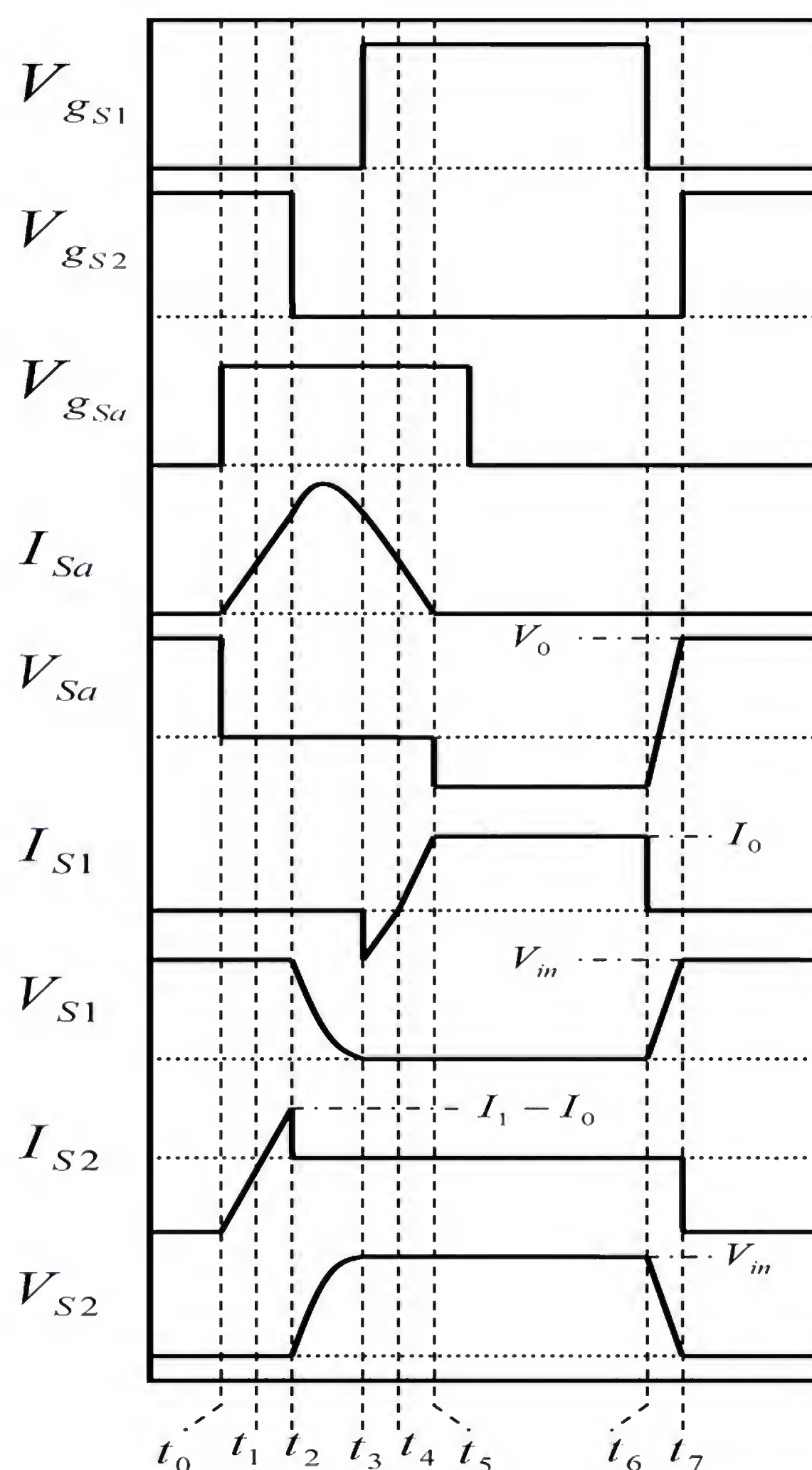


Figure 2: Main Theoretical Waveform of ZVT Buck Converter with SR

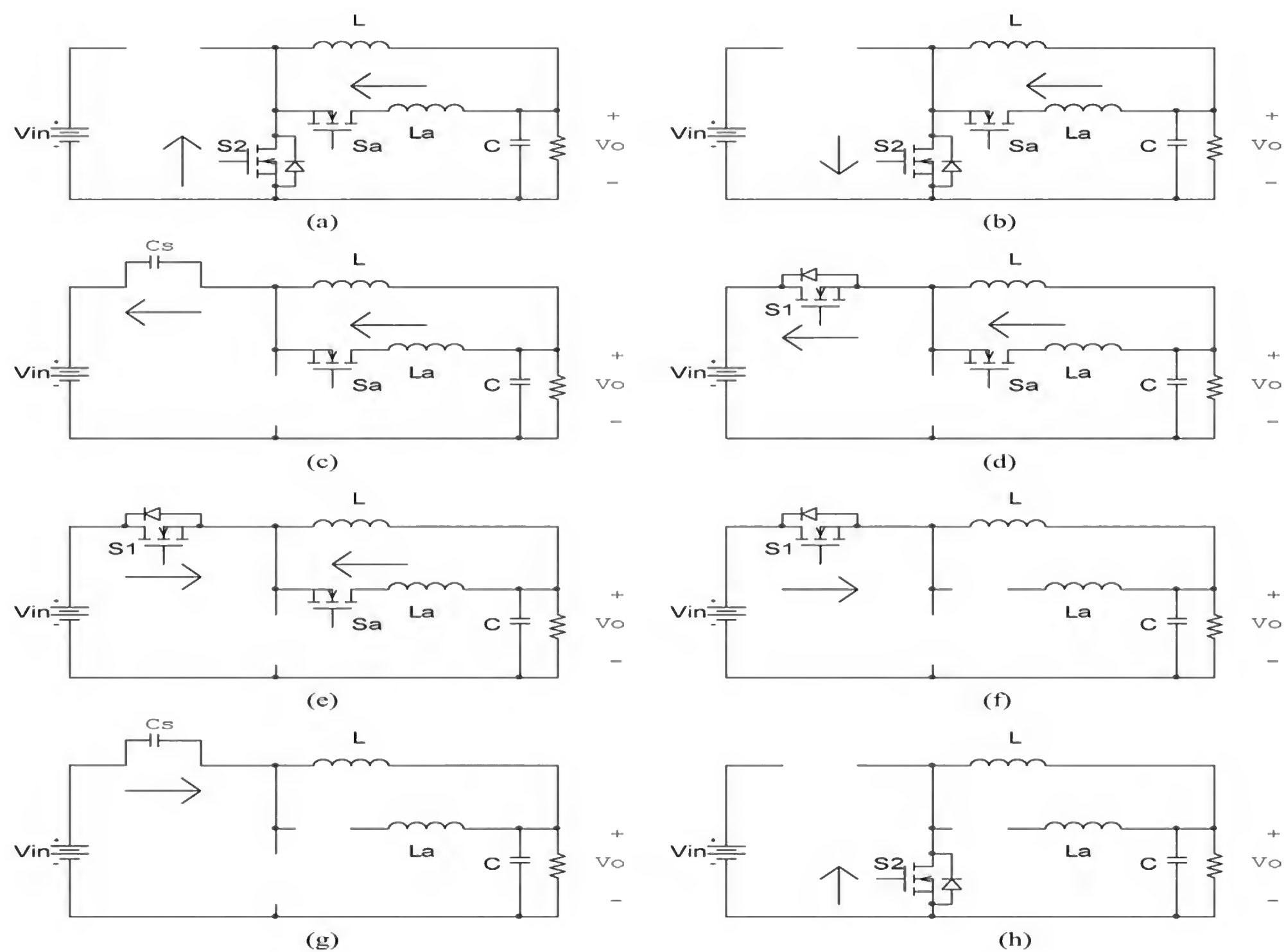


Figure 3: Equivalent Circuit for Each Operating Interval

Interval 4 [t_2-t_4]: In this interval, the body diode of S1 starts to conduct and C_s voltage remains zero. During this interval, L_a current decreases linearly to I_o and S1 can be turned on under ZVS.

Interval 5 [t_4-t_5]: In this interval, the main switch is ON, therefore, the difference of input and output voltages are placed across L_a . Since the output voltage is constant and input voltage is almost constant in a switching cycle, L_a current decreases linearly from I_o to zero, and accordingly, the main switch current increases from zero to I_o .

Interval 6 [t_5-t_6]: In this interval, S1 is ON and the converter behaves like a regular PWM buck converter.

Interval 7 [t_6-t_7]: This interval starts by turning S1 off. Due to C_s , S1 turns off under ZVS. In this interval, C_s is charged with constant current I_o until its voltage reaches V_{in} and S2 voltage reaches zero.

Interval 8 [t_7-t_0+T]: The S2 body diode starts to conduct and S2 can be turned on under Zero Voltage Switching condition.

III. DESIGN CONSIDERATIONS

Synchronous buck converter can be designed like a regular buck converter.

Input voltage = 80V

Output voltage = 40V

Output current = 2A

Switching frequency = 100 kHz

Duty ratio = 0.5

$$\text{Inductor value; } L = \frac{V_o(1-D)}{\Delta i_L f_{sw}} = 1\text{mH}$$

$$\text{Output Capacitor value; } C = \frac{\Delta i_L}{8\Delta V_o f_{sw}} = 5\mu\text{F}$$

Load resistance = 20 Ω

Power = 80 W

For ZVT buck converter with synchronous rectifier, capacitor Cs and auxiliary inductor La has to be designed. Capacitor Cs is the snubber capacitor for main switch and synchronous rectifier. Its value can be designed like any snubber capacitor. Inductor La is the snubber inductor of the auxiliary switch and its value can be designed like any turn on snubber inductor.

$$\text{Snubber Capacitance; } C_s = \frac{i_L t_f}{2V_{in}} = 0.25\text{nF}$$

$$\text{Auxiliary inductance; } L_a = \frac{V_{in} t_r}{2i_L} = 0.9\mu\text{F}$$

For MOSFET IRF540,

Rise time; $t_r = 45\text{ ns}$ and Fall time; $t_f = 20\text{ns}$.

IV. SIMULATION RESULTS

In order to analyse the working and advantages of the proposed ZVT buck converter with synchronous rectifier, the circuit is simulated using MATLAB/SIMULINK.

(1) Open Loop Operation

The simulation set up for ZVT synchronous buck converter in open loop mode is shown in Figure 4

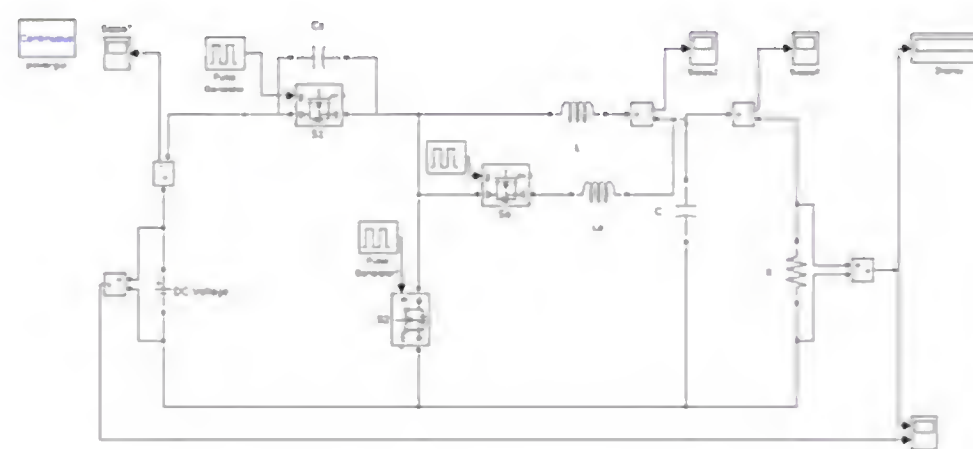


Figure 4: ZVT Synchronous Buck Converter

The switching frequency is 100 kHz and duty cycle is 0.5. The input voltage is 80V and output voltage is 40V. The output current is 2 A. Figure 5 and 6 shows the output current and output voltage waveform of ZVT synchronous buck converter. Figure 7 shows the voltage across synchronous rectifier.

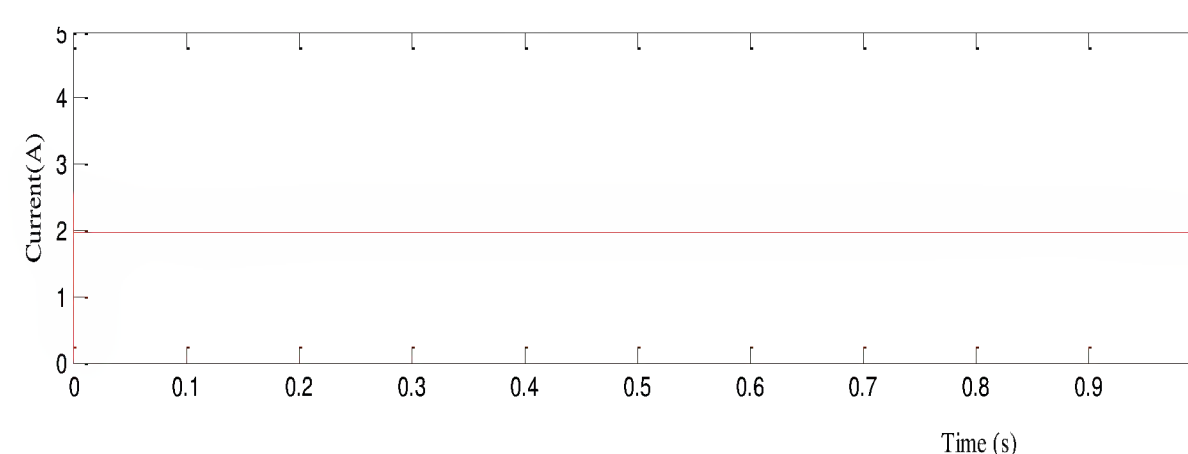


Figure 5: Output Current

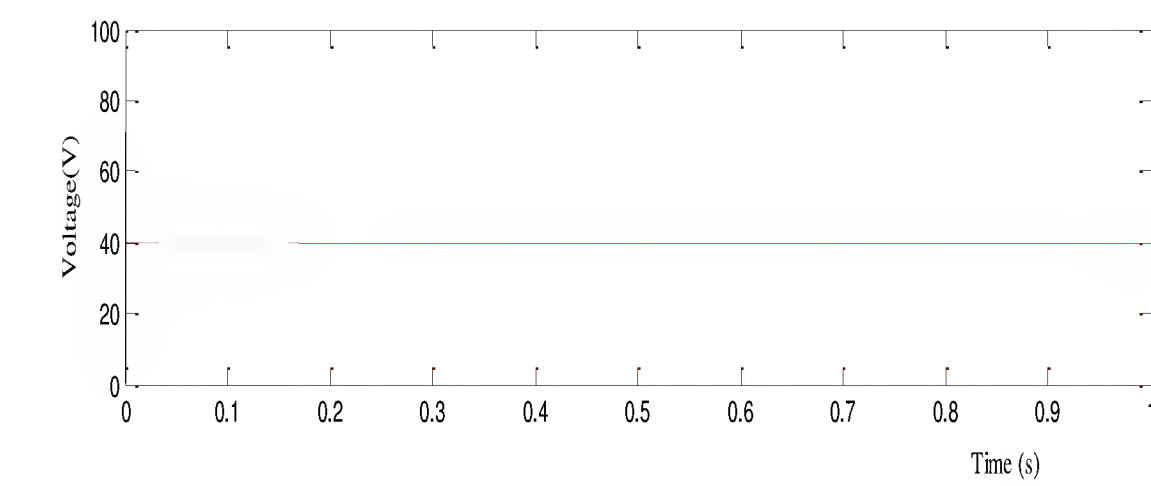


Figure 6: Output Voltage

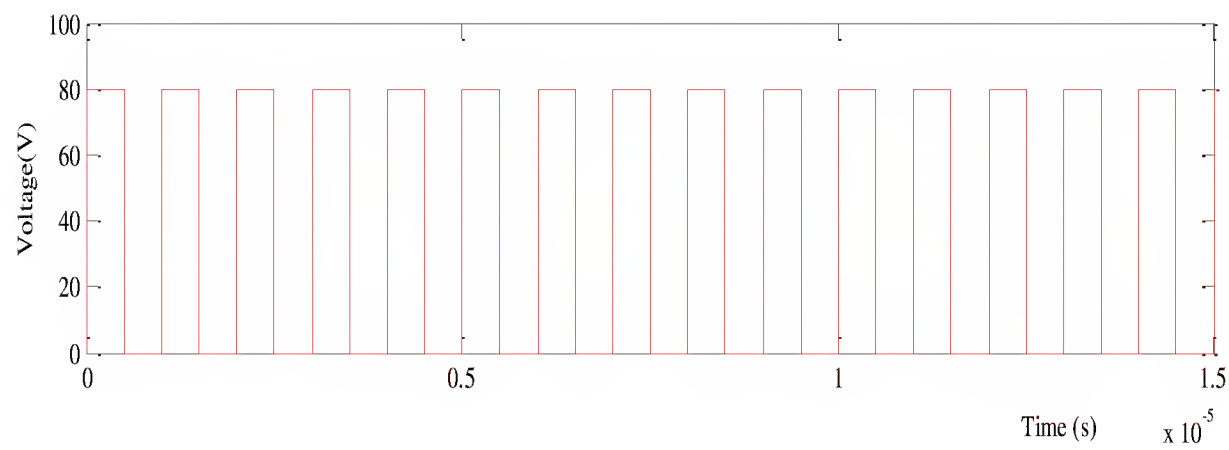


Figure 7: Synchronous Rectifier Voltage

In this proposed converter the main switch and synchronous rectifier is operated at ZVS condition and auxiliary switch at ZCS condition. To ensure this the gate pulses and voltage and current waveforms are compared. In Figure 8 and 9 gate pulses and main switch and synchronous rectifier voltages are compared. In Figure 8 gate pulses and auxiliary switch current is compared.

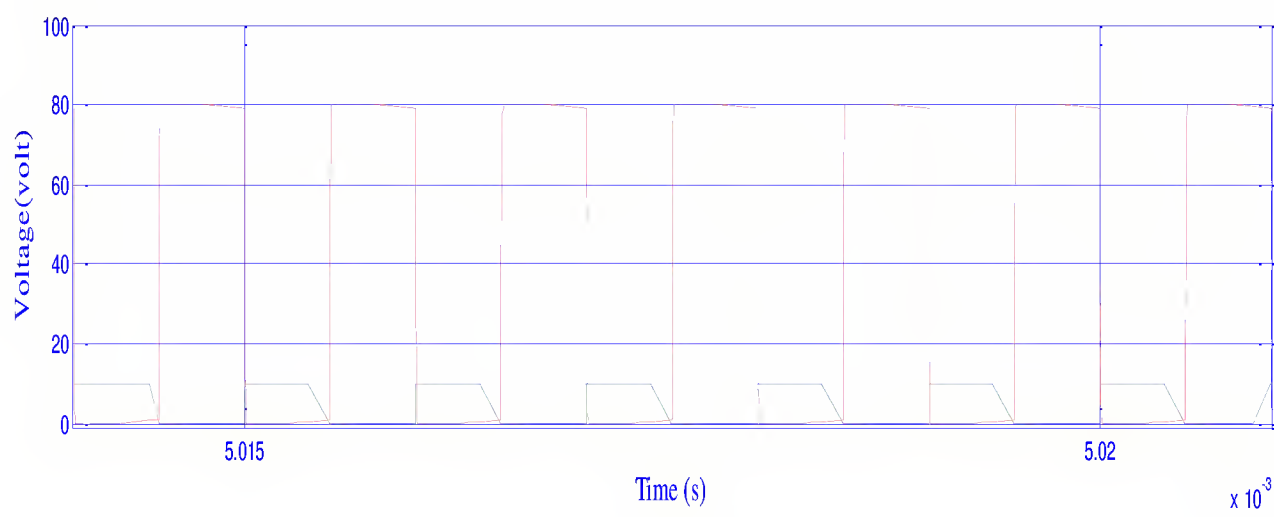


Figure 8: Main Switch Voltage and Gate Pulses

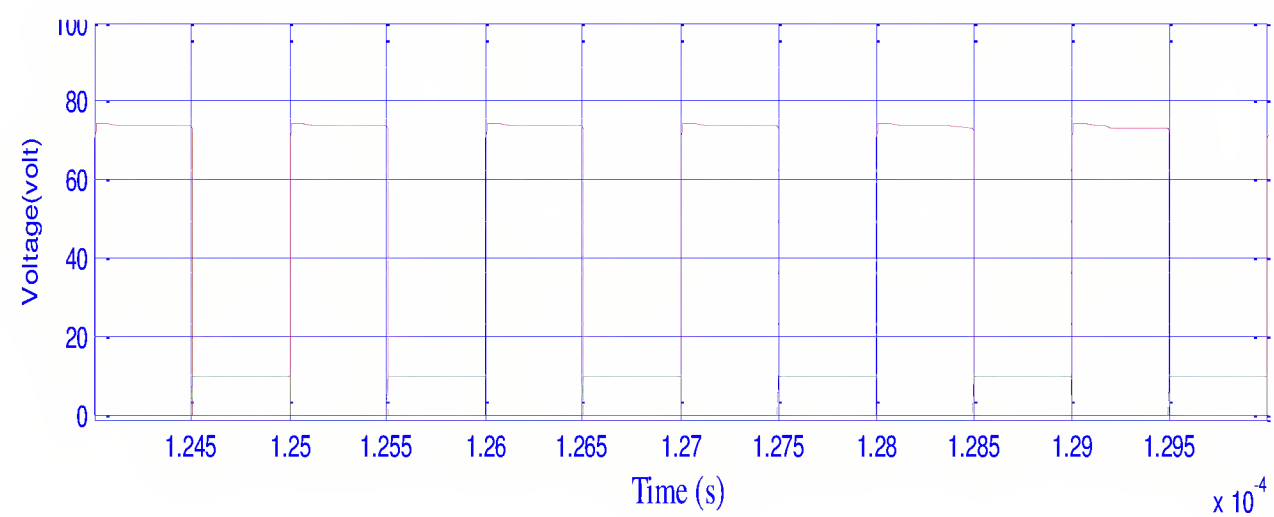


Figure 9: SR Voltage and Gate Pulse

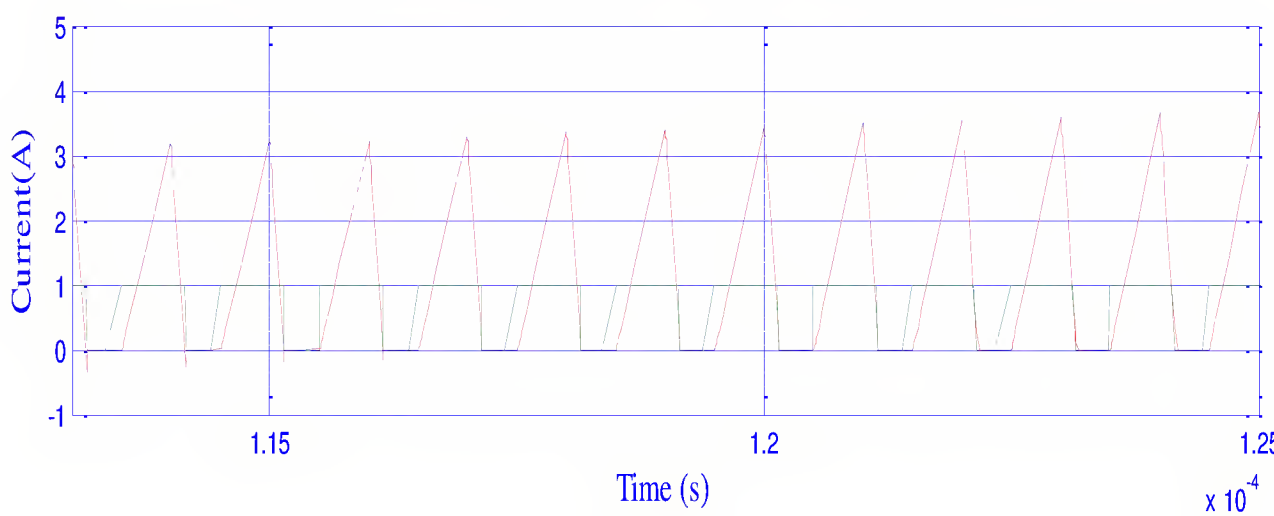


Figure 10: Auxiliary Switch Current and Gate Pulse

Conventional buck converter and synchronous buck converter with hard switching are simulated for the same specifications and the efficiency of three different topologies are compared in table 1. Figure 11 and 12 shows the simulation circuit of conventional and synchronous buck converter. Figure 13 shows the efficiency graph of three topologies.

Conduction loss across the rectifying diode in a conventional buck converter

$$P_D = V_O(1 - D)I_O = 0.7W$$

Conduction loss across SR in Synchronous buck converter

$$P_{SW} = I_O^2 R_{DS(on)}(1 - D) = 0.11W$$

Thus power loss is reduced in synchronous buck converter. So its efficiency is improved.

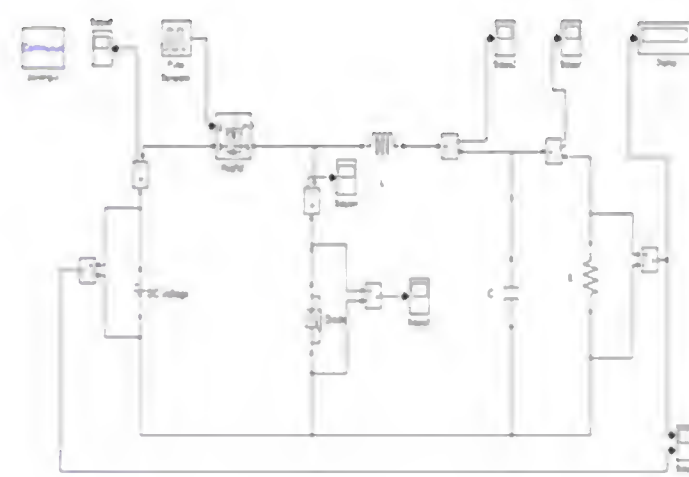


Figure 11: Conventional Buck Converter

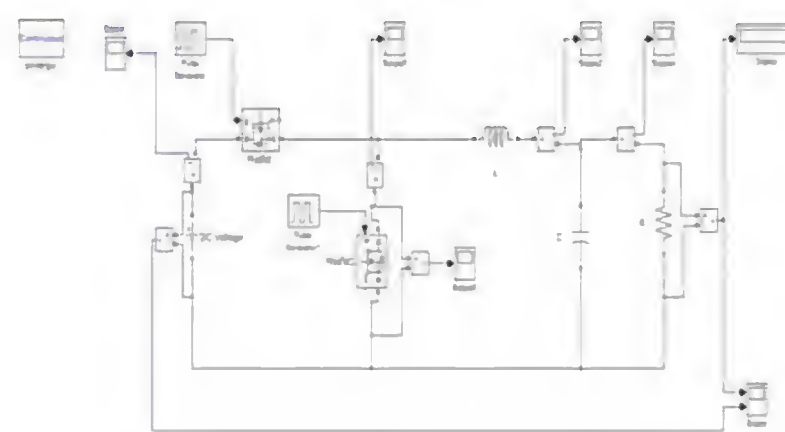


Figure 12: Synchronous Buck Converter

Table 1: Efficiency Comparison of Three Buck Converter Topologies

Converter	Input Vol. (V)	Output Vol. (V)	Input Cur. (A)	Output Cur (A)	η (%)
Conventional buck	80	39.5	1.05	1.98	92.7
Synchronous buck	80	39.62	1.03	1.97	94.86
ZVT buck with SR	80	39.74	0.99	1.94	96.7

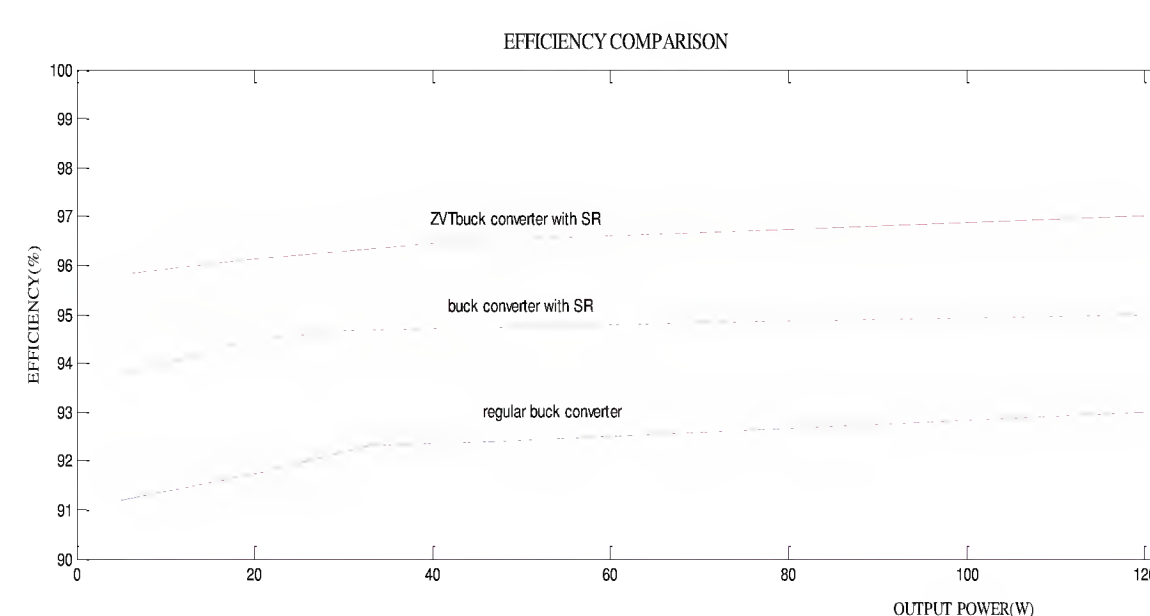


Figure 13: Efficiency Graph

(2) Closed Loop Operation

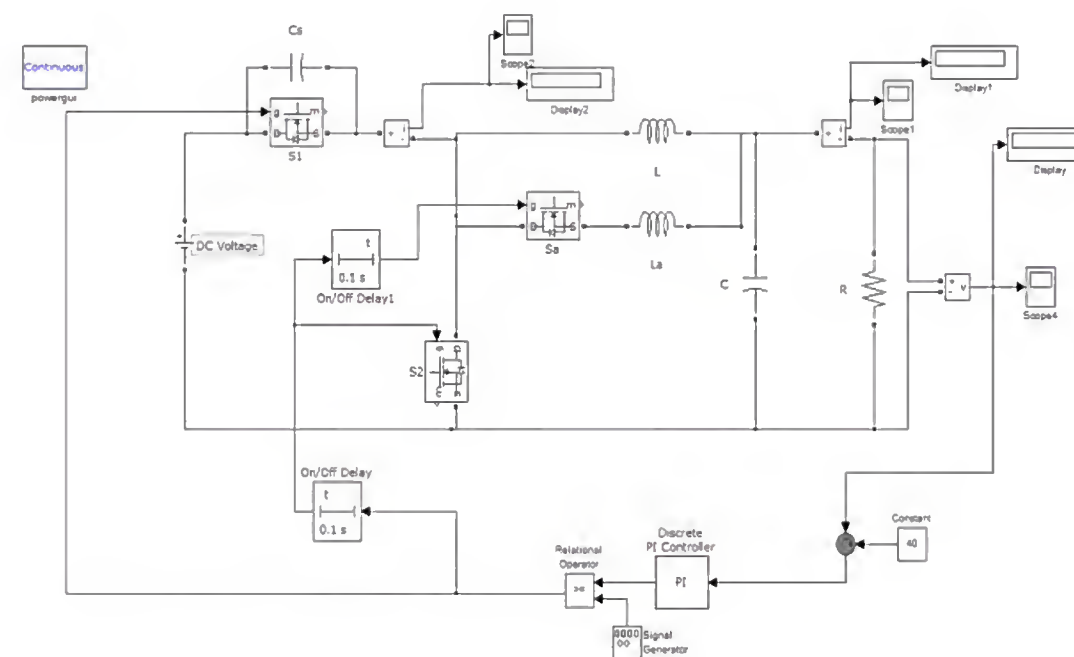


Figure 14: Closed Loop Operation of ZVT Buck Converter with SR

Figure 14 shows the simulation setup for closed loop operation of ZVT buck converter with synchronous rectifier. For the variation of input voltage from 45V to 80V the output remains constant at 40V. Figure 15 and Figure 16 shows the output voltage 40V for input voltages 45V and 80V.

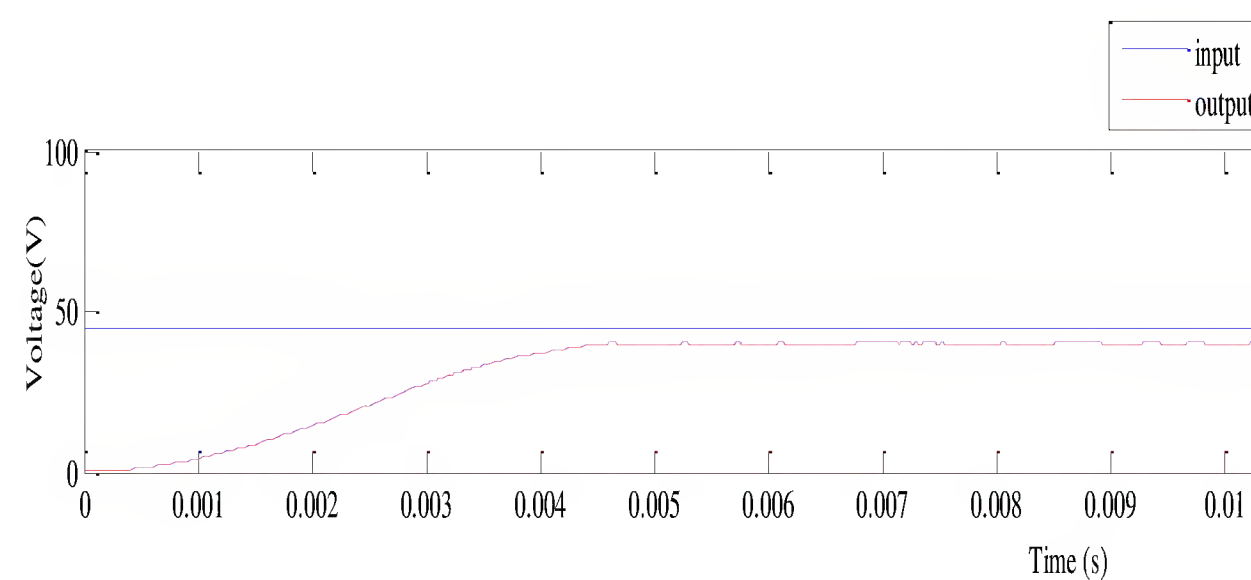


Figure 15: Output 40V for an Input 45V

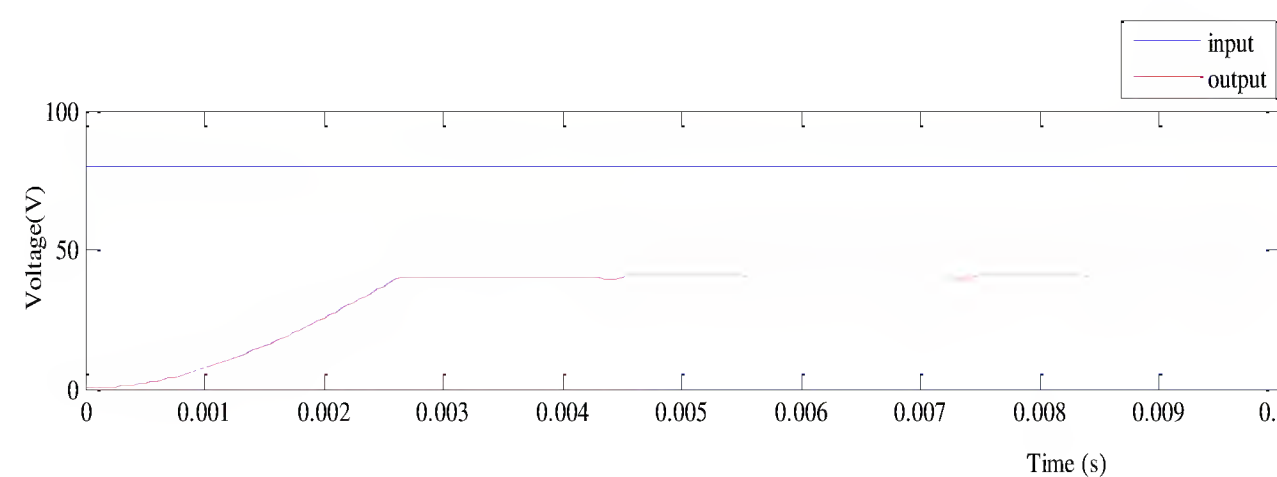


Figure 16: Output 40V for an Input 80V

V. CONCLUSIONS

In this paper, ZVT buck converter with SR was analyzed and simulated. This converter topology is compared with conventional buck converter and synchronous buck converter. The efficiency of ZVT buck converter is improved (about 97%) compared to other topologies. Applying SR to ZVT converters reduces the conduction losses and also results in wide soft switching range. This ZVT technique can be applied to other PWM converters also. The closed loop operation of ZVT synchronous buck converter is also performed.

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